REMARKS

The Official Action dated February 8, 2006 has been received and its contents noted. The Examiner is thanked for reviewing this application.

As previously, claims 1-5 are presently pending in the instant application, of which claim 1 is independent.

With reference now to the Official Action, the title of the invention stands objected to as not descriptive. In response, Applicants have replaced the current title with a new title, as shown above.

Claim 1 stands rejected under 35 U.S.C. §103(a) as unpatentable over Ibaraki (U.S. Patent No. 5,617,476) in view of well known prior art. Further, claims 2-4 stand rejected under 35 U.S.C. §103(a) as unpatentable over Ibaraki in view of previously cited Ahamed et al. (U.S. Patent No. 5,978,831 – hereafter Ahamed). Finally, claim 5 stands rejected under 35 U.S.C. §103(a) as unpatentable over Lyons further in view of Durkos. These rejections are respectfully traversed at least for the reasons provided below.

As the Examiner can readily appreciate, the present invention as set forth in independent claim 1, is directed to an image processing apparatus including at least two signal processor modules interconnected with each other in series, each of these signal processor modules having an input port through which data is input, a memory which stores data, a signal processor portion which carries out processing on input data according to a program and an output port through which data is output, wherein at least one of the signal processor modules outputs in parallel both unprocessed input data and processed data obtained by processing the input data.

Ibaraki, on the other hand, discloses an encryption device 223' in Fig. 8A having a separator 81 that receives sample data and separates the data into unprocessed portions and processed portion based on a processing flag information and masking signal provided to the separator. The portions of the data to be processed are transmitted to block encryption device 82 and eventually to synthesizer 83. The unprocessed portions (i.e., portions not to be encrypted) that have been separated from the processed portions (i.e., portions to be encrypted) are fed into the synthesizer 83 without being encrypted. For detailed description of Fig. 8A, the Examiner is invited to review col. 12, lines 28-41 of Ibaraki, which is shown below for Examiner's convenience:

> FIG. 8A is a block diagram of an encryption device 223' which is a modification of that shown in FIG. 3, and applies block encryption. As shown in FIG. 8A, this encryption device 223 comprises a separator 81, block encryption device 82, and synthesizer 83. The audio signal, process flag, and masking signal are input to the separator 81, which outputs as processed data the data of the position where the masking signal is `1` when the process flag of the sample data is `1`, and outputs the remaining data as unprocessed data. The block encryption device 82 then encrypts and outputs the processed data. The synthesizer 83 then synthesizes the unprocessed data and the output from the block encryption device 82; this operation is controlled by inputting the process flag and the masking signal to the synthesizer 83 to inverse the operation of the separator 81.

Clearly, Ibaraki does not teach, disclose or suggest least one of the signal processor modules outputs in parallel both unprocessed input data and processed data obtained by processing the input data, as recited in Applicants' claim 1. Rather, Ibaraki takes input data and divides the data into unprocessed portions and processed portions based on flag and masking information provided to the separator 81.

Moreover, the Examiner erroneously equated the separator 81 and block encryption device 82 of Ibaraki to Applicants' signal processor modules interconnected in series. Although the separator 81 and block encryption device 82 of Ibaraki are in part in series, the separator 81 is merely a data separator that separates sample data so that portions that are flagged are encrypted by the block encryption device 82.

Still further, the Examiner asserted that it is well known in the art that a function block that performs computer functions can have memory for storing program and a processor for executing program, and that it would have been obvious that function blocks 81 and 82 of Ibaraki be implemented including memory including program and processors to run program. In response, Applicants respectfully request the Examiner submit proper evidence supporting the improper assertion that the separator 81 and block encryption device each has a memory and a signal processor portion which carries out processing on input data according to a program.

Moreover, Applicants' respectfully assert that the separator 81 of Ibaraki is not a signal processor and there is no reason for the separator of Ibaraki to have its own memory and signal processor. Further, there is no reason to consider the separator 81 as a signal

processor when the block encryption device 82 is also considered by the Examiner as a signal processor.

The arguments set forth in relation to the rejection of claim 1 are also applicable to the rejection of its dependent claims.

With reference to the rejection of claims 2-4 over Ibaraki in view of U.S. Patent No. 5,978,831 to Ahamed, Applicants respectfully assert that Ahamed does nothing to overcome the aforementioned shortcomings associated with the teachings of Ibaraki.

In rejecting applicants' claimed invention, the Examiner notes that Ibaraki fails to specifically teach the input, processing and output as being controlled synchronously within cycles. Although Ahamed may set forth such a teaching, it is respectfully submitted that Ahamed fails to disclose that at least one of the signal processor modules outputs both unprocessed input data and processed data obtained by processing the input data as specifically recited by Applicants' claimed invention. That is, Ahamed does not cure the above discussed deficiencies of Ibaraki. Accordingly, it is respectfully submitted that Applicants' claimed invention as set forth in independent claim 1 as well as dependent claims 2-4 clearly distinguish over the combination proposed by the Examiner and are in proper condition for allowance.

With reference the rejection of claim 5 over Lyons in view Durkos, Applicants note that the Examiner remarked in the rejection of claim 5 in Section 7, page 6 of the Office Action that Lyon was discussed "above" with respect to claim 1. However, Lyon was not applied and discussed in the rejection of claim 1 in the Office Action mailed February 8, 2006. Rather, this rejection appears to be taken directly from or a repeat of the rejection of claim 5 in section 7, pages 6-7 in the Office Action mailed July 13, 2005. In response to this rejection, Applicants respectfully resubmit the arguments presently previously.

Again, Lyons fails to disclose or suggest that the signal processor outputs in parallel both unprocessed input data and processed data obtained by processing the input data, as recited in Applicants' claim 1. Particularly, it is noted that the decoder 136 of Lyons outputs one of the unprocessed input data and processed data. That is, the Lyons reference discloses outputting either the unprocessed input data or the processed data. As noted in col. 3, lines 40-42 of Lyons "the decode processor of 136 receives and processes the delivered data stream S8 and passes the processed or unprocessed data stream S9 to the transmitter."

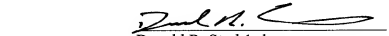
Clearly, the decoder 136 outputs only one kind of data and not in parallel of both the unprocessed input data and processed input data as is set forth in accordance with Applicants' claimed invention.

Furthermore, while Durkos may disclose a system with multiple functional modules for performing computing tasks, this references fails to disclose or suggest that the signal processor outputs both unprocessed input data and processed data obtained by processing the input data. Accordingly, it is respectfully submitted that Applicants' claimed invention as set forth in dependent claim 5 which includes all the limitations of independent claim 1 clearly distinguishes over the combination proposed by the Examiner.

Therefore, in view of the foregoing it is respectfully requested that the objections and rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-5 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,



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